STIC Search Report
EIC 2800

STIC Database Tracking Number: 162262

TO: Matthew Warren
Location: JEF-6C61
Art Unit: 2815
Tuesday, August 30, 2005

Case Serial Number: 10/734419

From: MARY S. MIMS
Location: STIC-EIC2800
JEF-4B59
Phone: 25928
Email: Mary.Mims@uspto.gov

Search Notes

Examiner Matthew Warren,

Please find attached results of your search for 10/724,419. The search was conducted using the CAS & Dialog databases relevant to semiconductors. The marked items appear to be the closest items located during our search. Please review all of the items presented

Based on this, if you have questions or would like a refocused search, please contact me. Thanks

Mary S. Mims

162262

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**
Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 8/11/05 Serial # 10/734419 Priority Application Date 12/4/95

Your Name Matthew Warren Examiner # 76062

AU 2815 Phone 571-272-1737 Room 6 C61

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ✓ Other _____
Secondary Refs ✓ Foreign Patents ✓
Teaching Refs ✓

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Invention pertains to a semiconductor assembly having 3 insulation layers & a photoresist. Silicon oxide (SiO), Silicon nitride (SiN), and Silicon Oxynitride (SiON), and then photoresist are stacked in that order. The SiON layer may also be an oxidized SiN layer. The most important thing is to find the film stack of SiO, SiN, SiON, & photoresist.

Staff Use Only
Searcher: Mary Mims
Searcher Phone: 25928
Searcher Location: STIC-EIC2800, JEF-4B68
Date Searcher Picked Up: 8/11/05
Date Completed: 8/30/05
Searcher Prep/Rev Time: 23 hr
Online Time: 15 1/2 hr

Type of Search
Structure (#)
Bibliographic ✓
Litigation
Fulltext ✓
Patent Family
Other

Vendors
STN ✓
Dialog
Questel/Orbit
Lexis-Nexis
WWW/Internet ✓
Other

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact:***

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

  Types of relevant prior art found:
  - ☐ Foreign Patent(s)
  - ☐ Non-Patent Literature
    (journal articles, conference proceedings, new product announcements etc.)
- *Relevant prior art **not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

sira Search and Information Resources Administration

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=> d his full

     (FILE 'HOME' ENTERED AT 09:17:35 ON 26 AUG 2005)

     FILE 'CAPLUS' ENTERED AT 09:18:11 ON 26 AUG 2005
               RECALL MARYJ MARYJ/L
               ---------
L1   (       428)SEA ABB=ON  PLU=ON  "N O SI"/ELF
L2   (       407)SEA ABB=ON  PLU=ON  N.O.SI/MF
L3   (       831)SEA ABB=ON  PLU=ON  "N SI"/ELF
L4   (         3)SEA ABB=ON  PLU=ON  "N4 SI3"/MF
L5   (         0)SEA ABB=ON  PLU=ON  N4 O2 SI3/MF
L6   (        48)SEA ABB=ON  PLU=ON  "O2 SI"/MF
L7   (       382)SEA ABB=ON  PLU=ON  O.SI/MF
L8   (     21767)SEA ABB=ON  PLU=ON  "O SI"/ELF
L9   (     92822)SEA ABB=ON  PLU=ON  PHOTO(A)(RESIST? OR MASK? OR LITHO? OR
               ENGRAV?) OR PHOTOLITHOG? OR PHOTOMASK? OR PHOTORESIST? OR
               LIGHT(2A)RESIST?
L10  (      2332)SEA ABB=ON  PLU=ON  (OXIDAT? OR LOCOS OR OXIDIS? OR OXIDIZ?)(L)
               (L3 OR L4)
L11  (       108)SEA ABB=ON  PLU=ON  L10 AND L9
L12  (        69)SEA ABB=ON  PLU=ON  L11(L)L6
L13  (        69)SEA ABB=ON  PLU=ON  L11 AND L6
L14  (   3566716)SEA ABB=ON  PLU=ON  ?LAYER? OR ?FILM? OR ?COAT? OR LAMINAT###
               OR DEPOSI?
L15  (        64)SEA ABB=ON  PLU=ON  L14 AND L13
L16  (   1704385)SEA ABB=ON  PLU=ON  THICK#### OR "NM" OR NANO(W)METER OR
               NANOMETER OR "AA" OR "ANG" OR ANGSTROM OR THIN(2A)FILM? OR
               ULTRATHIN OR ULTRA(W)THIN
L17  (        22)SEA ABB=ON  PLU=ON  L15 AND L16
L18  (         0)SEA ABB=ON  PLU=ON  L13 AND (L1 OR L2)
L19  (         0)SEA ABB=ON  PLU=ON  L11 AND (L1 OR L2)
L20  (       611)SEA ABB=ON  PLU=ON  (L1 OR L2) AND (L3 OR L4) AND (L7 OR L8)
L21  (        44)SEA ABB=ON  PLU=ON  L20 AND L9
L22  (        41)SEA ABB=ON  PLU=ON  L21 AND L14
L23  (        41)SEA ABB=ON  PLU=ON  L22 NOT L17
L24  (       170)SEA ABB=ON  PLU=ON  (L3 OR L4)(L)OXIDIZ?
L25  (       170)SEA ABB=ON  PLU=ON  OXIDIZ?(L)((L3 OR L4))
L26  (      6863)SEA ABB=ON  PLU=ON  SION OR (SI OR SILICON)(W)(OXIDE(W)NITRIDE
               OR OXYNITRIDE)
L27  (       308)SEA ABB=ON  PLU=ON  (L1 OR L2)(L)L26
L28  (     87498)SEA ABB=ON  PLU=ON  (OXIDED? OR OXIDI? OR OXYGEN#### OR "O" OR
               "O2")(1A)SIN OR SI3N4 OR SILICONITRIDE OR SILICON(W)NITRIDE OR
               SI(W)NITRIDE
L29  (     30831)SEA ABB=ON  PLU=ON  (L27 OR L28) AND (L3 OR L4) AND (L6 OR L7
               OR L8)
L30  (      3524)SEA ABB=ON  PLU=ON  L29 AND L9
L31  (      3227)SEA ABB=ON  PLU=ON  L30 AND L14
L32  (       778)SEA ABB=ON  PLU=ON  L31 AND L16
L33  (    343659)SEA ABB=ON  PLU=ON  SIMICONDUCT? OR WAFER OR IC OR SEMI(W)CONDU
               CT? OR CHIP OR MICRO(W)CHIP OR MICROCHIP OR INTEGRATED(W)CIRCUI
               T OR TRANSISTOR
L34  (       387)SEA ABB=ON  PLU=ON  L32 AND L33
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L35         6870 SEA ABB=ON  PLU=ON  SION OR (SI OR SILICON)(W)(OXIDE(W)NITRIDE
               OR OXYNITRIDE)
L36          758 SEA ABB=ON  PLU=ON  (OXIDED? OR OXIDI? OR OXYGEN#### OR "O" OR
               "O2")(1A)(SIN OR SI3N4 OR SILICONITRIDE OR SILICON(W)NITRIDE
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08/26/2005 Warren 10/734,419

```
               OR SI(W)NITRIDE)


     FILE 'REGISTRY' ENTERED AT 09:36:37 ON 26 AUG 2005
L37          428 SEA ABB=ON  PLU=ON  "N O SI"/ELF
L38          407 SEA ABB=ON  PLU=ON  N.O.SI/MF
L39          831 SEA ABB=ON  PLU=ON  "N SI"/ELF
L40            3 SEA ABB=ON  PLU=ON  "N4 SI3"/MF
L41           48 SEA ABB=ON  PLU=ON  "O2 SI"/MF
L42          382 SEA ABB=ON  PLU=ON  O.SI/MF
L43        21774 SEA ABB=ON  PLU=ON  "O SI"/ELF

     FILE 'CAPLUS' ENTERED AT 09:37:47 ON 26 AUG 2005
L44        92876 SEA ABB=ON  PLU=ON  (PHOTO(A)(RESIST? OR MASK? OR LITHO? OR
                 ENGRAV?)) OR PHOTOLITHOG? OR PHOTOMASK? OR PHOTORESIST? OR
                 LIGHT(2A)RESIST?
L45         2333 SEA ABB=ON  PLU=ON  (L39 OR L40)(L)(OXIDAT? OR LOCOS OR
                 OXIDIS? OR OXIDIZ?)
L46         3432 SEA ABB=ON  PLU=ON  (L37 OR L38)(L)L26
L47         1331 SEA ABB=ON  PLU=ON  (L39 OR L40) AND (L41 OR L42) AND (L46 OR
                 L36)
L48          187 SEA ABB=ON  PLU=ON  L47 AND L44
L49          184 SEA ABB=ON  PLU=ON  L48 AND L14
L50           49 SEA ABB=ON  PLU=ON  L49 AND L16
                 D 1-25 IBIB AB
                 D IBIB AB 26-49
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L17 ANSWER 20 OF 22 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1986:489712 CAPLUS
DOCUMENT NUMBER: 105:89712
TITLE: Semiconductor device manufacture
INVENTOR(S): Kayama, Shigeki; Hoshi, Naoya; Aoyama, Junichi; Shimada, Takashi
PATENT ASSIGNEE(S): Sony Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 61070736	A2	19860411	JP 1984-192094	19840913
PRIORITY APPLN. INFO.:			JP 1984-192094	19840913

AB A method for manufacturing semiconductor devices involves: (a) forming an insulating **layer** (especially SiO2) on a p-type substrate; (b) forming an oxidation-resistant **layer** (especially Si3N4) on the SiO2 insulator **layer**; (c) creating a **photoresist** mask on the oxidation-resistant **layer**; (d) reactive-ion etching of the insulating and oxidation-resistant **layers** in the desired shape; (e) injecting impurity ions (e.g., of B) into the top portion of the substrate not covered by the insulating **layer**; (f) forming a polycryst. Si **layer** by chemical vapor **deposition** over the entire surface of the device; (g) forming a **thick** SiO2 **layer** and a P+-type channel-stopper **layer** beneath it through thermal oxidation using the Si3N4 oxidn-resistant **layer** as a mask, and (h) etching the oxidation-resistant **layer** and a SiO2 **layer** formed on it during the thermal oxidation process. The method prevents the formation of a bird's beak during the thermal oxidation, since the polycryst. Si **layer** controls the bending of the Si3N4 oxidation-resistant **layer**.

L23 ANSWER 13 OF 41 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2000:570165 CAPLUS
DOCUMENT NUMBER: 133:143452
TITLE: Formation of an isolation **film** for a semiconductor device
INVENTOR(S): Hwang, Hyun-sang
PATENT ASSIGNEE(S): Lg Semiconductor Co., Ltd., S. Korea
SOURCE: Repub. Korea, No pp. given
CODEN: KRXXFC
DOCUMENT TYPE: Patent
LANGUAGE: Korean
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 9710151	B1	19970621	KR 1994-5629	19940321
PRIORITY APPLN. INFO.:			KR 1994-5629	19940321

AB The separation **film** of semiconductor element is formed as the following. (a) On the Si substrate, form the thin oxide **film** and the nitride **film** in that order and then through the **photo engraving** process using the active mask, remove the nitride **film** of field region and the oxide **film** in order. After that, the SiOxNy **layer** is formed by thermal processing it in NH3 atm or injecting N ion on the exposed substrate. (b) On the front side of the resulting material, form the polycryst. Si **film** and form the polycryst. Si sidewall on the sidewalls of nitride **film** and the oxide **film** through dry etching.

L23 ANSWER 17 OF 41 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2000:180926 CAPLUS
DOCUMENT NUMBER: 132:230643
TITLE: Semiconductor device including an antireflective etch stop **layer**
INVENTOR(S): Wang, Fei; Foote, David K.; Cagan, Myron R.; Gupta, Subhash
PATENT ASSIGNEE(S): Advanced Micro Devices, USA
SOURCE: U.S., 14 pp., Cont.-in-part of U.S. 5,710,067.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 6
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6040619	A	20000321	US 1997-937774	19970925
US 5710067	A	19980120	US 1995-479718	19950607
WO 9916118	A1	19990401	WO 1998-US17884	19980828
W: JP, KR				
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
EP 1034564	A1	20000913	EP 1998-943453	19980828
R: DE, FR, GB, NL				
JP 2001517870	T2	20011009	JP 2000-513315	19980828
US 6313018	B1	20011106	US 2000-504449	20000216
PRIORITY APPLN. INFO.:			US 1995-479718 A2	19950607
			US 1997-937774 A	19970925
			WO 1998-US17884 W	19980828

AB A microelectronic device such as a MOS transistor is formed on a semiconductor substrate. A W damascene interconnect for the device is formed using an etch stop **layer** of Si nitride, Si oxynitride, or Si oxime having a high Si content of .apprx.40-50 weight%. The etch stop **layer** has high etch selectivity relative to overlying insulator materials such as SiO2, tetraethylorthosilicate (TEOS) glass, and borophosphosilicate glass (BPSG). The etch stop **layer** also has a high index of refraction and is antireflective, thereby improving critical dimension control during **photolithog**. imaging.

REFERENCE COUNT: 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 46 OF 49 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1985:54778 CAPLUS
DOCUMENT NUMBER: 102:54778
TITLE: Isolation in fabrication of integrated circuits
INVENTOR(S): Sawada, Shizuo; Higuchi, Takayoshi
PATENT ASSIGNEE(S): Toshiba Corp., Japan
SOURCE: Ger. Offen., 37 pp.
CODEN: GWXXBX
DOCUMENT TYPE: Patent
LANGUAGE: German
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 3418638	A1	19841122	DE 1984-3418638	19840518
JP 59214237	A2	19841204	JP 1983-88573	19830520
PRIORITY APPLN. INFO.:			JP 1983-88573 A	19830520

AB A method for forming highly integrated circuits with isolation regions without bird beaks consists of **coating** Si with SiO2, Si3N4, poly-Si, and a **photoresist** mask, selectively etching a window through the **layers**, etching a groove in the Si substrate, removing the resist, thermally **oxidizing**, **depositing** **Si3N4**, **depositing** SiO2, masking, etching the SiO2 **layer**, selectively etching the Si3N4 **layer**, etching the underlying oxide and poly-Si **layers**, forming a field SiO2 **film**, and forming device components in the isolation region. Thus, p--Si(100) was thermally oxidized to .apprx.500 .**ANG**., a Si3N4 **film** .apprx.1200 .**ANG**. **thick** was **deposited**, poly-Si .apprx.300 .**ANG**. was **deposited**, a mask was applied, the underlying **layers** were reactive-ion etched using C2F6, the Si substrate was etched in KOH solution, 100-keV B+ ions were implanted to a dose of .apprx.1013 cm-2, the mask was removed, the exposed Si was thermally oxidized to 500 . **ANG**., Si3N4 **films** of 200 .**ANG**. and SiO2 **films** of 3000 .**ANG**. were **deposited**, the SiO2 **layer** was reactive-ion etched in C2F6, the exposed Si3N4 was etched using the SiO2 **layer** as a mask, the exposed SiO2 was etched in NH4F solution, the surface was thermally oxidized in steam at 1000° to give an .apprx.7000 .**ANG**. SiO2 field **film** and activate the B dopant, the 1st and 2nd Si3N4 **films** were removed, and the rest of the device components were completed.

L50 ANSWER 47 OF 49 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1984:482652 CAPLUS
DOCUMENT NUMBER: 101:82652
TITLE: Thin dielectric insulation in a silicon semiconductor
INVENTOR(S): Greschner, Johann; Trumpp, Hans Joachim
PATENT ASSIGNEE(S): IBM Deutschland G.m.b.H., Fed. Rep. Ger.
SOURCE: Ger. Offen., 40 pp.
CODEN: GWXXBX
DOCUMENT TYPE: Patent
LANGUAGE: German
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 3242113	A1	19840524	DE 1982-3242113	19821113
EP 111086	A2	19840620	EP 1983-109945	19831005
EP 111086	A3	19860730		
EP 111086	B1	19890308		
R: DE, FR, GB, IT, NL				
US 4502914	A	19850305	US 1983-546612	19831028
JP 59107518	A2	19840621	JP 1983-212610	19831114

PRIORITY APPLN. INFO.: DE 1982-3242113 A 19821113
EP 1983-109945 A 19831005

AB A method for forming a SiO2 isolation region of width .apprx.1 μ and depth .apprx.5 μ in a Si substrate consists of **coating** Si with a **thin** SiO2 **film**, **coating** with a resist, **coating** with Si3N4, **coating** with a **photoresist**, masking, reactive-ion etching 1st with O2 followed by CF4 and then **O2**, **depositing Si3N4**, reactive-ion etching off the top **layer** of Si3N4, reactive-ion etching the resist, **coating** with a sensitive resist, etching with CF4 plasma to remove the Si3N4 walls and etching down to the Si, etching into the Si with Cl2-Ar or O2 plasmas, thermally oxidizing or filling with oxide, nitride and a plastic, and reactive-ion etching in CHF3.

INSPEC

8/29/2005 Warren 10/734,419

Ref Items Index-term
E1- 4 CI=SI3N4O SS; E2- 2 CI=SI3N4O SUR; E4-1 CI=SI3N4O7
E5-1 CI=SI3N4O7 SS; E6-1 CI=SI3N4O7 SUR
S1
E3-73769 *CI=SIO2; E5-53822 CI=SIO2 BIN; E7-1 CI=SIO2 EL
E8-27605 CI=SIO2 INT; E9-26091 CI=SIO2 SS
S2
E1-7 SI3N; E3-60 *SI3N4
S3
E3-9267 *CI=SI3N4; E5-9215 CI=SI3N4 BIN; E7-3974 CI=SI3N4 INT
E8-64 CI=SI3N4 SS; E9-1705 CI=SI3N4 SUR
S4
E3-1911 *CI=SION; E6-1061 CI=SION INT; E7-1911 CI=SION SS
E8-168 CI=SION SUR; E20-1 CI=SION-SI-SIO2 INT
S5
E3-73769 *CI=SIO2; E5-53822 CI=SIO2 BIN; E7-1 CI=SIO2 EL
E8-27605 CI=SIO2 INT; E9-26091 CI=SIO2 SS; E10-14710 CI=SIO2 SUR
S6
E3-4249 *CI=SIN; E5-4231 CI=SIN BIN; E7-2234 CI=SIN INT
E9-460 CI=SIN SUR
S7
E3-3474 *CI=SIO; E5-3441 CI=SIO BIN; E7-1229 CI=SIO INT
E8-38 CI=SIO SS; E9-491 CI=SIO SUR
S8
R2-921 F 1 LOCOS; R14-16529 R 56 SEMICONDUCTOR TECHNOLOGY
R15- 24293 R 17 SURFACE CHEMISTRY; R16-17918
R-25 SURFACE TREATMENT; R19-48090 ; R-16 CC=B2550E Surface treatment (semiconductor technology)
S9

File 2:INSPEC 1969-2005/Aug W2
(c) 2005 Institution of Electrical Engineers

Set Items Description
S1 5 E1,E2,E4,E5,E6
S2 73769 E3,E5,E7,E8,E9
S3 67 E1,E3
S4 9267 E3,E5,E7,E8,E9
S5 1911 E3,E6,E7,E8,E20
S6 73769 E3,E5,E7,E8,E9,E10

S7 4249 E3,E5,E7,E9
S8 3474 E3,E5,E7,E8,E9
S9 94911 R2,R14,R15,R16,R19
S10 22223 TRISILICON()TETRANITRIDE OR SILICON()NITRIDE OR "SIN" OR S-
ILICONITRIDE OR SI()NITRIDE
S11 118215 DIOXOSILICON? ? OR SILICONDIOXIDE? ? OR SILICON()DIOXIDE? ?
OR SILICON()OXIDE? ? OR SILICA? ? OR "SIO" OR "SIO2"
S12 2336 SILICON()OXYNITRIDE? ? OR "SION" OR ((SI OR SILICON)()(OXI-
DE? ?()NITRIDE? ?))
S13 69911 PHOTO? ?(A)(RESIST???? OR MASK??? OR LITHOG????? OR ENGRAV-
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PHOTOENGRAV???
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OR "ANG" OR ANGSTROM OR THIN(2N)FILM? ? OR ULTRATHIN OR ULTR-
A()THIN
S15 1000839 LAYER??? OR FILM? ? OR COAT??? OR LAMINAT??? OR DEPOSI????
S16 83979 OXIDAT????? OR LOCOS OR OXIDIS???? OR OXIDIZ?????
S17 480 (S1 OR S5 OR S12) AND (S3 OR S4 OR S7 OR S10) AND (S2 OR S-
11 OR S6 OR S8)
S18 17 S17 AND S13

18/5/12
DIALOG(R)File 2:INSPEC

4827224 INSPEC Abstract Number: B9501-2550E-003
Title: Computer-controlled plasma etching and endpoint detection in GaAs device processing
Author(s): Chen Zhengming
Author Affiliation: Nanjing Electron. Devices Inst., China
Journal: Research & Progress of SSE vol.14, no.2 p.182-5
Publication Date: May 1994 Country of Publication: China
CODEN: GDYJE2 ISSN: 1000-3819
Language: Chinese Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: The research on plasma etching with NF/sub 3//N/sub 2/ shows that high etching rates and good etching uniformities for materials such as SiO/sub 2/, SiON, Si/sub 3/N/sub 4/, WN and W at low RF power, with thin masked AZ1518 photoresist, can be obtained. A variety of RF parameters during the etching processing have been applied to monitor and control the plasma etching with computer technology. (4 Refs)
Subfile: B
Descriptors: gallium arsenide; III-V semiconductors; semiconductor technology; sputter etching
Identifiers: computer control; endpoint detection; GaAs device processing ; masked AZ1518 photoresist; RF power; computer monitoring; plasma etching; NF/sub 3//N/sub 2/; GaAs; NF/sub 3/; N/sub 2/; SiO/sub 2/; SiON; Si/sub 3/N/sub 4/; WN; W
Class Codes: B2550E (Surface treatment for semiconductor devices); B2520D (II-VI and III-V semiconductors)
Chemical Indexing:
GaAs sur - As sur - Ga sur - GaAs bin - As bin - Ga bin (Elements - 2)
NF3 bin - F3 bin - F bin - N bin (Elements - 2)
N2 el - N el (Elements - 1)
SiO2 sur - O2 sur - Si sur - O sur - SiO2 bin - O2 bin - Si bin - O bin (Elements - 2)
SiON sur - Si sur - N sur - O sur - SiON ss - Si ss - N ss - O ss (Elements - 3)
Si3N4 sur - Si3 sur - N4 sur - Si sur - N sur - Si3N4 bin - Si3 bin - N4 bin - Si bin - N bin (Elements - 2)
WN sur - N sur - W sur - WN bin - N bin - W bin (Elements - 2)
W sur - W el (Elements - 1)

18/5/13
DIALOG(R)File 2:INSPEC

03931952 INSPEC Abstract Number: A91099321, B91049744
Title: Chemical etching of thermally oxidized silicon nitride: comparison of wet and dry etching methods
Author(s): Loewenstein, L.M.; Tipton, C.M.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Journal: Journal of the Electrochemical Society vol.138, no.5 p. 1389-94
Publication Date: May 1991 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: The ability to etch silicon nitride changes after this material is exposed to a wet oxygen ambient, as a result of the partial oxidation of the silicon nitride to form a silicon oxynitride. The authors have measured the etch rate of silicon nitride exposed to different oxidation temperatures and pressures, to determine how these parameters affect the mask removal step needed in the local oxidation of silicon-based processing sequence. Both wet (hydrofluoric acid and phosphoric acid) and dry (SF/sub 6/-based remote plasma) isotropic etch methods are described, and correlated to Rutherford backscattering and ellipsometric measurements. The results show the presence of an oxidized layer which increased in thickness with oxidation temperature and pressure. Process modifications must comprehend the altered silicon nitride surface in order to adequately strip this film. (9 Refs)
Subfile: A B
Descriptors: ellipsometry; etching; oxidation; Rutherford backscattering; semiconductor technology; silicon compounds
Identifiers: chemical etching; wet etching; oxidation pressure; thermally oxidized; dry etching; oxidation temperatures; isotropic etch; Rutherford backscattering; ellipsometric measurements; Si/sub 3/N/sub 4/; SiO/sub x/N/sub y/
Class Codes: A8160C (Semiconductors); A7920N (Atom, molecule, and ion impact); B2550E (Surface treatment and oxide film formation)
Chemical Indexing:
Si3N4 sur - Si3 sur - N4 sur - Si sur - N sur - Si3N4 bin - Si3 bin - N4 bin - Si bin - N bin (Elements - 2)
SiON ss - Si ss - N ss - O ss (Elements - 3)

18/5/17
DIALOG(R)File 2:INSPEC

02049010 INSPEC Abstract Number: A83052965, B83030117
Title: Comments on: 'Chemical conversion of composite films on silicon by electron beam irradiation'
Author(s): Heimann, R.B.
Author Affiliation: Inst. for Materials Res., McMaster Univ., Hamilton, Ont., Canada
Journal: Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena) vol.1, no.1 p.108-10
Publication Date: Jan.-March 1983 Country of Publication: USA
CODEN: JVTBD9 ISSN: 0734-211X
U.S. Copyright Clearance Center Code: 0734-211X/83/010108-03$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: New Developments (N); Practical (P); Experimental (X)
Abstract: The process described has potential application for the fabrication of integrated circuits by bypassing photolithographic techniques. The formation of silicon nitride or silicon oxynitride by electron beam-activated reaction of ammonia with silicon oxide is essentially topotactical and ensures a selective masking on a microscopical to submicroscopical scale. Exposure time can be drastically reduced by using high-energy radiation, such as laser beams. Nonconverted films are readily dissolved away by buffered hydrofluoric acid whereas the silicon nitride is not affected by this treatment. Advantages of this novel process may lie in the LTV (low temperature vapor) deposition of surface films thus preventing introducing of lattice defects and undesired out diffusion and precipitation of dopant atoms owing to the high temperatures required for the current fabrication process. (15 Refs)
Subfile: A B
Descriptors: chemical vapour deposition; electron beam effects; insulating thin films; integrated circuit technology; radiation chemistry; silicon compounds
Identifiers: Si/sub 3/N/sub 4/ film; insulating film; SiO/sub 2/+NH/sub 3/; SiO/sub x/N/sub y/ film; low temperature; vapour deposition; composite films; fabrication; integrated circuits; electron beam-activated reaction; selective masking
Class Codes: A6855 (Thin film growth, structure, and epitaxy); A8115H (Chemical vapour deposition); A8250 (Photochemistry and radiation chemistry); B0520F (Vapour deposition); B2520C (Elemental semiconductors); B2550E (Surface treatment and oxide film formation); B2550G (Lithography); B2570 (Semiconductor integrated circuits)

File 6:NTIS 1964-2005/Aug W2

File 8:Ei Compendex(R) 1970-2005/Aug W2

File 34:SciSearch(R) Cited Ref Sci 1990-2005/Aug W3

File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

File 35:Dissertation Abs Online 1861-2005/Aug

File 23:CSA Technology Research Database 1963-2005/Jul

File 36:MetalBase 1965-20050825

File 65:Inside Conferences 1993-2005/Aug W3

File 92:IHS Intl.Stds.& Specs. 1999/Nov

File 94:JICST-EPlus 1985-2005/Jul W1

File 99:Wilson Appl. Sci & Tech Abs 1983-2005/Jul

File 103:Energy SciTec 1974-2005/Aug B1

File 144:Pascal 1973-2005/Aug W2

File 239:Mathsci 1940-2005/Oct

File 305:Analytical Abstracts 1980-2005/Aug W2

File 315:ChemEng & Biotec Abs 1970-2005/Jul

File 347:JAPIO Nov 1976-2005/Apr(Updated 050801)

File 350:Derwent WPIX 1963-2005/UD,UM &UP=200554

Set	Items	Description
S1	556058	PHOTO(A)(RESIST???? OR MASK???? OR LITHOG????? OR ENGRAV??-??) OR PHOTORESIST???? OR PHOTOMASK???? OR PHOTOLITHO???? OR -PHOTOENGRAV????
S2	242464	TRISISLICON()TETRANITRIDE OR SILICON()NITRIDE? ? OR "SIN" -OR SILICONITRIDE? ? OR SI()NITRIDE? ?
S3	1006135	DIOXOSILICON OR SILICONDIOXIDE OR SILICON()DIOXIDE OR SILI-CON()OXIDE OR SILICA OR "SIO" OR "SIO2"
S4	14554	SILICON()OXYNITRIDE OR "SION" OR ((SI OR SILICON)()(OXIDE(-)NITRIDE))
S5	654	S1 AND S2 AND S3 AND S4
S6	4787394	THICK???? OR "NM" OR NANO()MEETER? ? OR NANOMETER? ? OR "A-A" OR "ANG" OR ANGSTROM? ? OR THIN(2N)FILM? ? OR ULTRATHIN OR ULTRA()THIN???
S7	382	S5 AND S6
S8	373	RD (unique items)
S9	9982614	LAYER???? OR FILM? ? OR COAT???? OR LAMINAT???? OR DEPOSI?-????
S10	375	S7 AND S9
S11	3899831	SEMICONDUCT???? OR WAFER? ? OR "IC" OR SEMI()CONDUCT???? OR CHIP OR MICRO()CHIP? ? OR MICROCHIP? ? OR INTEGRATED()CIRCU-

08/29/2005 Warren 10/734,419

IT? ? OR TRANSISTOR? ?

S12	314	S10 AND S11
S13	57071890	PY<1995
S14	16	S12 AND S13

14/5/1 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1518555 NTIS Accession Number: DE90618522
Ion beam studied of silicon oxynitride and silicon nitroxide thin layers (Proefschrift (Dr))
Oude Elferink, J. B.
Utrecht Rijksuniversiteit (Netherlands).
Corp. Source Codes: 019965000; 5526800
Report No.: INIS-MF-12525
11 Oct 89 121p
Languages: English Document Type: Thesis
Journal Announcement: GRAI9019
Includes summary in Dutch.

NTIS Prices: PC A06/MF A01
Country of Publication: Netherlands
In this the processes occurring during high temperature treatments of silicon oxynitride and silicon oxide layers are described. Oxynitride layers with various atomic oxygen to nitrogen concentration ration (O/N) are considered. The high energy ion beam techniques Rutherford backscattering spectroscopy, elastic recoil detection and nuclear reaction analysis have been used to study the layer structures. A detailed discussion of these ion beam techniques is given. Numerical methods used to obtain quantitative data on elemental compositions and depth profiles are described. The electrical compositions and depth profiles are described. The electrical properties of silicon nitride films are known to be influenced by the behaviour of hydrogen in the film during high temperature anneling. Investigations of the behaviour of hydrogen are presented. Oxidation of silicon (oxy)nitride films in O(sub 2)/H(sub 2)0/HCl and nitridation of silicon dioxide films in NH(sub 3) are considered since oxynitrides are applied as an oxidation mask in the LOCOS (Local oxidation of silicon) process. The nitridation of silicon oxide layers in an ammonia ambient is considered. The initial stage and the dependence on the oxide thickness of nitrogen and hydrogen incorporation are discussed. Finally, oxidation of silicon oxynitride layers and of silicon oxide layers are compared. (author). 76 refs.; 48 figs.; 1 tab. (Atomindex citation 21:025427)
Descriptors: *Silicon Nitrides; *Silicon Oxides; Thin Films; Experimental Data; Ion Beams; Nuclear Reaction Analysis; Proton Recoil Detectors; Rutherford Scattering; Tables(data)

14/5/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03508725 **Image available**
PATTERN FORMATION

PUB. NO.: 03-171625 [JP 3171625 A]
PUBLISHED: July 25, 1991 (19910725)
INVENTOR(s): NAKANO HIROBUMI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-311273 [JP 89311273]
FILED: November 29, 1989 (19891129)
INTL CLASS: [5] H01L-021/302; G03F-007/26; H01L-021/338; H01L-029/812
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 29.1 (PRECISION INSTRUMENTS -- Photography & Cinematography)
JAPIO KEYWORD:R004 (PLASMA)
JOURNAL: Section: E, Section No. 1124, Vol. 15, No. 412, Pg. 89, October 21, 1991 (19911021)

ABSTRACT

PURPOSE: To enable a pattern in fine dimension below the resolving power limit to be formed by a method wherein the specific position of the first coating layer formed into the first pattern on a substrate is further coated with the second coating layer taking a taper protrusion shape.

CONSTITUTION: The first thin film 2 comprising SiO(sub 2) or SiON, etc., for a dummy pattern is deposited on a semiconductor substrate 1. Next, the first resist 3 is formed on the first thin film 2 by the ordinary photolithography. Next, the first thin film 2 is RIE processed using the first resist 3 as a mask which is removed to form the dummy pattern. Finally, the second thin film 4 comprising e.g. silicon nitride etc. is deposited by bias ECR plasma CVD process on the semiconductor substrate 1 containing the first thin film 2 so that the second thin film 4 on the first thin film 2 may take a taper protrusion shape.

14/5/8 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008029308 **Image available**
WPI Acc No: 1989-294420/198941
XRAM Acc No: C89-130367
XRPX Acc No: N89-224571
Device having silicon substrate with sunken field oxide regions - obtd. using mask of silicon oxynitride and silicon nitride to provide recesses in which field oxide regions are formed
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG)
Inventor: LIFKA H; WOERLEE P H
Number of Countries: 006 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 336515	A	19891011	EP 89200845	A	19890403	198941	B
NL 8800903	A	19891101				198946	
JP 2012822	A	19900117	JP 8185860	A	19810406	199009	
EP 336515	B1	20011017	EP 89200845	A	19890403	200169	
DE 68929332	E	20011122	DE 629332	A	19890403	200201	
			EP 89200845	A	19890403		

Priority Applications (No Type Date): NL 88903 A 19880408
Cited Patents: 3.Jnl.Ref; EP 166474; EP 189795; EP 208356; US 4038110

Abstract (Basic): EP 336515 A

Process is for the mfr. of a semiconductor device comprising a silicon substrate (1) with fully or partially sunken field oxide regions (7) for the mutual insulation of regions (8) where semiconductor elements are formed in the substrate. A mask is formed in a layer of silicon oxynitride (2) covering the substrate surface and an overlying layer of silicon nitride (3), and this mask is used to provide recesses in the substrate by carrying out a first oxidn. step and then etching away the silicon oxide thus formed. The ultimate field oxide regions are then formed in the recesses thus obtd. by a second oxidn. step while masking the mask.

Pref. the mask layers consist of 30 to 60 nm of silicon oxynitride and 50 to 200 nm of silicon nitride. The first layer of silicon oxide is etched away isotropically in a buffer soln. of hydrogen fluoride and ammonium fluoride.

USE/ADVANTAGE - For the mfr. of devices with a flat topography so that wiring tracks for interconnection of elements can be provided relatively easily on a flat surface. Produces an undergrowth of the field oxide regions which is smaller than that obtd. with known methods, and provides recesses which are more homogeneous and more accurate than previously possible. Since no chromium soln. is used to etch the silicon oxide, the ultimate device is of better quality than that obtd. using known methods.

Title Terms: DEVICE; SILICON; SUBSTRATE; SUNK; FIELD; OXIDE; REGION; OBTAIN ; MASK; SILICON; OXYNITRIDE; SILICON; NITRIDE; RECESS; FIELD; OXIDE; REGION; FORMING
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/762
International Patent Class (Additional): H01L-021/32; H01L-021/76
File Segment: CPI; EPI

14/5/11 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007189553
WPI Acc No: 1987-186562/198727
XRAM Acc No: C87-077674
XRPX Acc No: N87-139452

Simultaneous prodn. of self-aligned bipolar and CMOS transistors - on common silicon substrate by multi-stage deposition, structurising and doping

Patent Assignee: SIEMENS AG (SIEI)
Inventor: SCHABER H C; WIEDER A; BIEGER J

Number of Countries: 008 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 227970	A	19870708	EP 86116735	A	19861202	198727	B
JP 62155554	A	19870710	JP 86301096	A	19861216	198733	
US 4737472	A	19880412	US 86931640	A	19861117	198817	
EP 227970	B	19900808				199032	
DE 3673364	G	19900913				199038	

Priority Applications (No Type Date): DE 3544621 A 19851217
Cited Patents: 1.Jnl.Ref; EP 110313; EP 80523; EP 83785; FR 2531812

Abstract (Basic): EP 227970 A

Prodn. involves producing n-doped zones (5) in p-doped substrate (1) for p-channel transistors (c) and placing insulated npn-bipolar transistors (a) in n-doped zones (5), so that n-zones (5) form collector of transistor (A).

The process is as follows: (a) Prodn. of a double film of SiO2 and Si3N4 on a p-doped substrate (1) and structurisaion of the Si3N4 film by local oxidn. (LOCOS). (b) Prodn. of field oxide (3) for sepg. active transistor zones (A,B,C) in substrate (1) by local oxid., using Si3N4 structure as oxidn. mask. (c) Prodn. of n-zones (5) and p-zones (4) in substrate (1) by implantation of n- and p-doping ions respectively and diffusion. (d) removal of nitride/oxide mask. (e) Prodn. of 1st insulating film (6) with a thickness of max 50 nm over entire surface, which acts as protective film for later gate zones in etching and dielectric for the memory capacitors (D) and also prevents diffusion of B from p-conducting film (8) applied later into zones of bipolar transistors (A) adjacent to later collector zone (K). (f) Removal of this 1st insulating film (6) from all areas of later bipolar transistors (A) except collector zone (I) and adjacent areas by photolithography. (g) Removal of photoresist mask. (h) Implantation to dope electrodes (7) of memory capacitors (8) in substrate (A), using a photoresist technique. (i) Deposition of a p-conducting film (8) of poly-Si, metal silicide or a double film of poly-Si and metal silicide on entire surface. (j) Deposition of a second insulating film (9) on entire surface. (k) Structurisation of these 2 films (8,9) with vertical edges until substrate (1) is exposed by dry etching to define base zone of bipolar transistors (A) and memory capacitor zone (D).

USE/ADVANTAGE The process is used for producing VLSIs with high switching rates.

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Title Terms: SIMULTANEOUS; PRODUCE; SELF; ALIGN; BIPOLAR; CMOS; TRANSISTOR; COMMON; SILICON; SUBSTRATE; MULTI; STAGE; DEPOSIT; STRUCTURE; DOPE
Index Terms/Additional Words: COMPLEMENTARY; METAL; OXIDE; SEMICONDUCTOR;

14/5/13 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004505336
WPI Acc No: 1986-008680/198602
XRAM Acc No: C86-003656
XRPX Acc No: N86-006229

Mfr. of silicon body with sunken oxide layer - using two oxidn. masks, the second adjoining the first on sidewalls of a depression

Patent Assignee: PHILIPS GLOEILAMPENFAB NV (PHIG)
Inventor: BARTSEN J W; DIL J G
Number of Countries: 009 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 166474	A	19860102	EP 85200783	A	19850515	198602	B
NL 8401711	A	19851216	NL 841711	A	19840529	198603	
JP 60257538	A	19851219	JP 85112307	A	19850527	198606	
US 4622096	A	19861111	US 85729843	A	19850502	198648	
CA 1230428	A	19871215				198802	
CN 8501827	A	19870110				198806	
EP 166474	B	19881026				198843	
DE 3565910	G	19881201				198849	

Priority Applications (No Type Date): NL 841711 A 19840529
Cited Patents: 1.Jnl.Ref; A3...8827; DE 931556; FR 2243523; GB 2048435; JP 58156783; US 2011035; US 2335814; US 3448765; US 3826280; US 4271583; US 4361280; US 4398992
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 166474	A	E	21		
Designated States (Regional): DE FR GB IT NL					
EP 166474	B	E			
Designated States (Regional): DE FR GB IT NL					

Abstract (Basic): EP 166474 A

Semiconductor device is formed by: forming an oxidn. mask on an Si body; forming a depression with sidewalls which are flat and enclose an angle of 25-45 deg. with the surface; forming a second oxidn. mask on the sidewalls of 5-50 nm thick Si (oxy)nitride applied directly or sepd. by an oxide layer of thickness below 5 nm; and carrying out an oxidn. treatment.

USE/ADVANTAGE - In mfr. of semiconductor devices contg. a large no. of circuit elements. A sunken oxide layer of very flat structure is formed in a simple, non-critical manner.

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Title Terms: MANUFACTURE; SILICON; BODY; SUNK; OXIDE; LAYER; TWO; OXIDATION ; MASK; SECOND; ADJOIN; FIRST; SIDEWALL; DEPRESS
Derwent Class: L03; P78; U11
International Patent Class (Additional): B44C-001/22; C03C-015/00; C03C-025/06; H01L-021/76
File Segment: CPI; EPI; EngPI

14/5/15 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003674944
WPI Acc No: 1983-34915K/198315
XRAM Acc No: C83-034095
XRPX Acc No: N83-063168
Forming oxide isolation regions in silicon - using nitride oxide mask with lateral edges of oxide converted to silicon oxynitride
Patent Assignee: GENERAL ELECTRIC CO (GENE)
Inventor: GHEZZO M; MCCONNELEE P A
Number of Countries: 006 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 75875	A	19830406				198315	B
JP 58074051	A	19830504				198324	
JP 90054657	B	19901122	JP 82169474	A	19820928	199051	

Priority Applications (No Type Date): US 81305883 A 19810928
Cited Patents: 2.Jnl.Ref; A3...8627; EP 6706; EP 71203; JP 57076856; No-SR.Pub; US 3874919; US 4113515; US 4272308
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 75875	A	E	13		

Designated States (Regional): DE FR GB IT NL

Abstract (Basic): EP 75875 A

Semiconductor substrate having an active region on its surface surrounded by SiO2 is made by (a) providing a first type substrate with an active region on its surface; (b) forming a thin SiO2 layer on the surface; (c) forming a thick Si3N4 layer on the SiO2; (d) patterning the Si3N4 to produce a retained portion (18) overlying and registered with the active region; (e) similarly patterning the SiO2, exposing the major substrate surface surrounding the active region; (f) converting the peripheral portions of the retained SiO2 into Si oxynitride; (g) converting the exposed substrate to SiO2 (14) by heating in an oxidising atmos.; and (h) removing retained portions of the Si3N4 and SiO2 overlying the active region.

Pref., the substrate is etched to a predetermined depth, esp. about 57% thickness SiO2 to be formed in (g), before (g), so the surface of substrate and grown oxide are coplanar.

Formation of Si oxynitride inhibits oxidn., maintaining the size of the active region and minimising 'bird's beak' formation, during formation of oxide isolation regions for ICs.

3D-F/3

Title Terms: FORMING; OXIDE; ISOLATE; REGION; SILICON; NITRIDE; OXIDE; MASK ; LATERAL; EDGE; OXIDE; CONVERT; SILICON; OXYNITRIDE
Derwent Class: L03; U11
International Patent Class (Additional): H01L-021/31
File Segment: CPI; EPI

14/5/16 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002485870
WPI Acc No: 1980-03887C/198003
Insulating films for silicon semiconductor devices - formed by nitriding a surface silicon dioxide film
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: ITO T; NOZAKI T
Number of Countries: 005 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 6706	A	19800109				198003 B
JP 54162967	A	19791225				198130
JP 81028017	B	19810629				198130
EP 6706	B	19851030				198544
DE 2967538	G	19851205				198550
US 4621277	A	19861104				198647
JP 54163679	A	19791226				199037
US 4980307	A	19901225	US 89401489	A	19890830	199103
EP 6706	B2	19930317	EP 79301114	A	19790612	199311

Priority Applications (No Type Date): JP 7872654 A 19780615; JP 7871618 A 19780614
Cited Patents: DE 1644012; GB 1234665; US 3520722; US 3798061; US 4056642; 1.Jnl.Ref; FR 2223836; DE 1489188; US 3385729
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 6706	A	E			
Designated States (Regional): DE GB NL					
EP 6706	B	E			
Designated States (Regional): DE GB NL					
EP 6706	B2	E	15	H01L-021/318	
Designated States (Regional): DE GB NL					

Abstract (Basic): EP 6706 A
In prodn. of a semiconductor device having an insulating film, an SiO2 film on an Si substrate is heated in a nitriding atmosphere to convert at least a portion of it to Si nitride. The SiO2 film is formed pref. by thermal oxidn. of the Si substrate.
In prodn. of gate insulator films of MISFET devices, capacitor dielectrics, passivation films or selective masks used in formation of semiconductor devices.
The nitrided SiO2 film is more dense than a vapour-deposited Si nitride film; also no sharp interface is formed between the nitride layer and the dioxide layer so that the no. of recombination centres is reduced.
Title Terms: INSULATE; FILM; SILICON; SEMICONDUCTOR; DEVICE; FORMING; NITRIDATION; SURFACE; SILICON; FILM
Derwent Class: L03; U11; U12
International Patent Class (Main): H01L-021/318
International Patent Class (Additional): H01L-021/28; H01L-021/31; H01L-021/314; H01L-029/46; H01L-029/62
File Segment: CPI; EPI